REMARKS

This is a full and timely response to the Office Action of June 3, 2003. Reexamination, reconsideration, and allowance of the application and all presently pending claims are respectfully requested.

Upon entry of this First Response, claims 1-21 are pending in this application. Claims 20 and 21 are newly added. Furthermore, the specification has been amended to comply with requirements made in the outstanding Office Action. It is believed that the foregoing amendments add no new matter to the present application.

Specification Objections

The disclosure was objected to because of informalities, and more specifically the Office Action requested clarification or correction to drawing reference numerals 112 and 177 on page 11, 12, 14, 15, and 19. Applicant submits that the specification has been amended, as suggested by the office action, such that it overcomes this objection. In view of the amendment, applicant requests that the objection to the specification be withdrawn. Applicant submits that the amendment to the specification is for purposes of clarification and that the amendment does not add new matter to the application.

Response to §102 Rejections

A proper rejection of a claim under 35 U.S.C. §102 requires that a single prior art reference disclose each element of the claim. See, *e.g.*, *W.L. Gore & Assoc., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 U.S.P.Q. 303, 313 (Fed. Cir. 1983).

Claim 1

Claim 1 is rejected under 35 U.S.C. §102 as being anticipated by *Novak et al.* Amended claim one reads as follows:

> 1. A computer system for efficiently executing instructions of computer programs, comprising:
> processing circuitry having a pipeline, said pipeline configured to execute instructions from one of a plurality of programs, said processing circuitry configured to stop executing said one program during a first context switch in response to a first context switch command and to resume executing said one program during a second context switch in response to a second context switch command;
> cache memory;
> computer memory having a plurality of addresses; and
> ***memory control circuitry coupled to said processing circuitry, said memory control circuitry, in response to said second context switch command, configured to identify one of said addresses of said computer memory that is storing a data value previously written by said pipeline during execution of an instruction of said one computer program prior to said first context switch, said memory control circuitry further configured to retrieve said data value from said computer memory in response to said second context switch command and to store said retrieved data value in said cache memory***. (Emphasis added).

Applicant respectfully asserts that *Novak et al.* fails to disclose at least the features of claim 1 highlighted hereinabove.

In this regard, *Novak et al.* appears to disclose a microprocessor that manages process switching by storing a unique process identification number (PID) in a "process identification register (PIDR)," and providing this PID with each instruction or data entry in cache. See *Novak et al.*, col. 8, lines 17-20. When a new process is initiated, it appears that the microprocessor in *Novak et al.* "stores the unique process identification number assigned to process 1" and "assigns a unique process identification number to process 2," which the microprocessor then stores in the PIDR

and provides with each instruction or data entry in cache associated with process 2. See *Novak et al.*, col. 8, lines 47-55.

Thus, in response to a context switch, the "microprocessor switches back to process 1," and "those instructions and data for process 1 that have not been replaced by instructions and data for process 2 remain in the cache and can be accessed, because the microprocessor will reload the unique process identification number for process 1 and that number will still be in the PID locations associated with process 1 instructions and data that have not been replaced by a subsequent process." See *Novak et al.*, col. 8, lines 57-65.

However, claim 1 specifically claims circuitry configured "to retrieve said data value from said computer memory in response to said second context switch command and to store said retrieved data value in said cache memory," wherein the data value is a value "**previously written by the pipeline** during execution of an instruction of said one computer program prior to said first context switch." Although it appears that the system of *Novak et al.* "stores the unique process identification number assigned to process 1" and "reload[s] the unique process identification number for process 1" into a process identification register (PIDR) in response to a context switch, it does not appear to disclose "retriev[ing] said data value...in response to said second context switch command," wherein the data value was "previously written by the pipeline during execution of an instruction." To the contrary, *Novak et al.* specifically discloses a system that relies on "data that [may or may not] have been replaced by a subsequent process" during execution of the another process. See *Novak et al.*, col. 8, lines 47-65. (Emphasis added). Whereas, claim 1 claims a system that "in response to said second context switch command...retrieve[s] said data value...previously written by said pipeline" and

""store[s] said retrieved value in said cache memory." It appears that the value disclosed in *Novak et al.* that is written into cache is not a "data value previously written by said pipeline," but "comprises a the value assigned to a process by the microprocessor." See Novak et al., col. 4, lines 57-59.

Thus, Applicant submits that *Novak et al.* fails to disclose at least the features of "memory control circuitry coupled to said processing circuitry, said memory control circuitry, in response to said second context switch command, configured to identify one of said addresses of said computer memory that is storing a data value previously written by said pipeline during execution of an instruction of said one computer program prior to said first context switch, said memory control circuitry further configured to retrieve said data value from said computer memory in response to said second context switch command and to store said retrieved data value in said cache memory." as claimed in claim 1.

For at least the above reasons, Applicant respectfully submits that *Novak et al.*. is inadequate to anticipate each feature of claim 1, and the 35 U.S.C. §102 rejection of claim 1 should, therefore, be withdrawn.

Claims 2-6

Claims 2 through 6 presently stand rejected in the Office Action under 35 U.S.C. §102 as allegedly being anticipated by *Novak et al.* Applicant submits that the pending dependent claims 2 through 6 contain all features of their respective independent claim 1. Since claim 1 should be allowed, as argued hereinabove, pending dependent claims 2 through 6 should be allowed as a matter of law for at least this reason. *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988).

Claim 7

Claim 7 is rejected under 35 U.S.C. §102 as being anticipated by *Novak et al.*

Claim one reads as follows:

> 7. A computer system for efficiently executing instructions of computer programs, comprising:
>
> processing circuitry having a pipeline, said pipeline configured to execute instructions from one of a plurality of programs, said processing circuitry configured to stop executing said one program during a first context switch in response to a first context switch command and to resume executing said one program during a second context switch in response to a second context switch command;
>
> cache memory;
>
> computer memory having a plurality of addresses; and
>
> ***memory control circuitry coupled to said processing circuitry, said memory control circuitry configured to maintain a plurality of mappings, said mappings respectively correlating data values previously written by said pipeline during execution of an instruction and stored in said cache memory with said memory addresses of said computer memory, said memory control circuitry configured to store said mappings in said computer memory in response to said first context switch command and to retrieve said data values from said addresses that are identified by said mappings stored in said computer memory in response to said second context switch command, said memory control circuitry further configured to store in said cache memory said retrieved data values.*** (Emphasis added).

For at least the reason set forth hereinabove with reference to claim 1, Applicant respectfully asserts that *Novak et al.* fails to disclose at least the features of claim 7 highlighted hereinabove.

Claims 8-11

Claims 8 through 11 presently stand rejected in the Office Action under 35 U.S.C. §102 as allegedly being anticipated by *Novak et al.* Applicant submits that the pending dependent claims 8 through 11 contain all features of their respective independent claim 7. Since claim 7 should be allowed, as argued hereinabove, pending dependent claims 8 through 11 should be allowed as a matter of law for at least this reason. *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988).

Claim 12

Claim 12 is rejected under 35 U.S.C. §102 as being anticipated by *Novak et al.* Claim one reads as follows:

> 12. A method for efficiently executing instructions of computer programs, comprising the steps of:
> executing a plurality of computer programs in an interleaved fashion;
> switching which of said computer programs is being executed in said executing step;
> ***storing, prior to said switching step, at an address in computer memory a data value previously written by a pipeline in execution of an instruction corresponding to one of said computer programs in said executing step;***
> ***identifying said address in response to said switching step;***
> ***retrieving said data value from said address based on said identifying step and in response to said switching step;***
> ***storing said retrieved data value in cache memory; and***
> ***retrieving said data value from said cache memory in response to said executing step.*** (Emphasis added)

For at least the reasons set forth hereinabove with reference to claim 1, Applicant respectfully asserts that *Novak et al.* fails to disclose at least the features of claim 12 highlighted hereinabove.

Claims 13-15

Claims 13 through 15 presently stand rejected in the Office Action under 35 U.S.C. §102 as allegedly being anticipated by *Novak et al.* Applicant submits that the pending dependent claims 13 through 15 contain all features of their respective independent claim 12. Since claim 12 should be allowed, as argued hereinabove, pending dependent claims 13 through 15 should be allowed as a matter of law for at least this reason. *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988).

Claim 16

Claim 16 is rejected under 35 U.S.C. §102 as being anticipated by *Novak et al.* Claim one reads as follows:

> 16. A method for efficiently executing instructions of computer programs, comprising the steps of:
> executing instructions from a computer program;
> halting said executing step during a first context switch in response to a first context switch command;
> resuming said executing step during a second context switch in response to a second context switch command;
> maintaining a plurality of mappings;
> ***correlating, via said mappings, data values previously written by a pipeline during the executing step and stored in a cache memory with memory addresses of computer memory outside of said cache memory;***
> ***storing said mappings in said computer memory in response to said first context switch command;***
> ***retrieving, based on said mappings and in response to said second context switch command, at least one data value from at least one of said addresses identified by said mappings; and***

storing said at least one retrieved data value in said cache memory. (Emphasis added)

Applicant respectfully asserts that *Novak et al.* fails to disclose at least the features of claim 16 highlighted hereinabove.

Claims 17-19

Claims 17 through 19 presently stand rejected in the Office Action under 35 U.S.C. §102 as allegedly being anticipated by *Novak et al.* Applicant submits that the pending dependent claims 17 through 19 contain all features of their respective independent claim 16. Since claim 16 should be allowed, as argued hereinabove, pending dependent claims 17 through 19 should be allowed as a matter of law for at least this reason. *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988).

Claim 20

Claim 20 is newly added and reads as follows:

> 20. (New) A computer system for efficiently executing instruction of computer programs, comprising:
> a processing unit;
> memory outside of the processing unit;
> logic configured to store in said memory outside of the processing unit a data value previously requested or previously written by an instruction of a first process being executed by the processing unit when the processing unit context switches out the first process for processing of a second process, the logic further configured to retrieve the data value and continue executing the first process with the retrieved data value when the processing unit context switches out the second process and context switches in the first process.

Applicant submits that claim 20 should be allowed for at least the reasons set forth hereinabove with reference to claim 1.

Claim 21

Claim 21 is newly added and reads as follows:

> 21. (New) A method for efficiently executing instructions of computer programs, comprising the steps of:
>
> storing in memory outside of a processing unit a data value previously requested or previously written by an instruction of a first process being executed by the processing unit when the processing unit context switches out the first process for processing of a second process;
>
> retrieving the data value when the processing unit context switches out the second process and context switches in the first process; and
>
> continuing execution of the first process with the data value retrieved in the retrieving step.

Applicant submits that claim 20 should be allowed for at least the reasons set forth hereinabove with reference to claim 1.

CONCLUSION

Applicant respectfully requests that all outstanding objections and rejections be withdrawn and that this application and all presently pending claims be allowed to issue. If the Examiner has any questions or comments regarding Applicant's response, the Examiner is encouraged to telephone Applicant's undersigned counsel.

Respectfully submitted,

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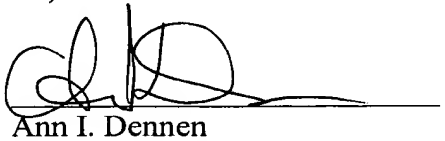
By: 

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